Amendments to the Claims

1. *(Currently Amended)* A method ~~(700)~~ for providing an external clock signal to an internal memory block of a self-timed memory comprising: receiving ~~(710)~~ an internal clock signal from a clock monitor of the self-timed memory; receiving ~~(720)~~ an external clock signal; receiving ~~(730)~~ a control signal; and, providing, in dependence upon the control signal ~~(740),~~ the internal clock signal to the internal memory block during a normal mode of operation ~~(750)~~ of the self-timed memory, and the external clock signal to the internal memory block during a test mode ~~(760)~~ of the self-timed memory.

2. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 wherein the external clock signal received during test mode is generated according to a predetermined test pattern.

3. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 2 wherein the external clock signal received during test mode comprises a duty cycle lower than a 50% duty cycle of the internal memory block.

4. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 2 wherein the external clock signal received during test mode comprises a duty cycle higher than a 50% duty cycle of the internal memory block.

5. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 wherein the internal clock signal is provided to the internal memory block in absence of a control signal.

6. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 wherein a control signal indicating initiation of the test mode is provided.

7. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 6 wherein a control signal indicating termination of the test mode is provided.

8. *(Original)* A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 7 wherein at least a control signal is provided during the test mode.

9. *(Currently Amended)* A self-timed memory comprising: an internal memory block ~~(150);~~ a clock monitor ~~(152)~~ for receiving an external clock signal and for providing an internal clock signal ~~(PHIX)~~ in dependence thereupon to the internal memory block; a test system ~~(100)~~ interposed between the clock monitor and the internal memory block, the test

system comprising: an internal clock signal input port ~~(PHIX)~~ in signal communication with the clock monitor ~~(152)~~ for receiving the internal clock signal ~~(PHIX)~~; an external clock signal ~~(CL)~~ input port for receiving the external clock signal; a control signal ~~(CS)~~ input port for receiving a control signal; an output port ~~(102)~~ in signal communication with the internal memory block; and, a multiplexer ~~(110)~~ in signal communication with the internal clock signal ~~(PHIX)~~ input port, the external clock signal input port ~~(CL)~~, the control signal input port ~~(CS)~~ and the output port, the control circuitry for receiving the internal clock signal, the external clock signal, and the control signal, and for providing, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal mode of operation of the self-timed memory, and for providing the external clock signal to the internal memory block during a test mode of the self-timed memory.

10. *(Original)* A self-timed memory as defined in claim 9 wherein the clock monitor comprises an input port for receiving the external clock signal and wherein the input port is connected to the external clock signal input port of the test system.

11. *(Original)* A self-timed memory as defined in claim 10 comprising test circuitry in signal communication with the test system, the test circuitry for providing a control signal to the test system and for providing the external clock signal to the test system during test mode.

12. *(Original)* A self-timed memory as defined in claim 9 wherein the internal memory block comprises an address decoder.

13. *(Original)* A self-timed memory as defined in claim 9 wherein the internal memory block comprises a sense amplifier.

14. *(Original)* A self-timed memory as defined in claim 9 wherein the internal memory block comprises a column and bank decoder

15. *(Original)* A self-timed memory as defined in claim 9 wherein the internal memory block comprises a precharge and discharge circuitry.

16. *(Original)* A self-timed memory as defined in claim 9 wherein the internal memory block comprises input/output latches.

17. *(Original)* A self-timed memory comprising: at least an internal memory block; a clock monitor for receiving an external clock signal and for providing at least an internal clock signal in dependence thereupon to the at least an internal memory block; a test system interposed between the clock monitor and the at least an internal memory block, the test system comprising: at least an internal clock signal input port in signal communication with the clock monitor for receiving at least an internal clock signal; an external clock signal input port for receiving the external clock signal; a control signal input port for receiving a control signal; at least an output port in signal communication with the at least an internal memory block; and, control circuitry in signal communication with the at least an internal clock signal

input port, the external clock signal input port, the control signal input port and the at least an output port, the control circuitry for receiving the at least an internal clock signal, the external clock signal, and the control signal, and for providing, in dependence upon the control signal, the at least an internal clock signal via the at least an output port to the at least an internal memory block during a normal mode of operation of the self-timed memory, and for providing the external clock signal to at least one of the at least an internal memory block during a test mode of the self-timed memory.

18. *(Original)* A self-timed memory as defined in claim 17 wherein the control circuitry comprises a multiplexer.

19. *(Original)* A self-timed memory as defined in claim 18 wherein the at least an internal memory block comprises an address decoder.

20. *(Original)* A self-timed memory as defined in claim 19 wherein the at least an internal memory block comprises a sense amplifier.

21. *(Original)* A self-timed memory as defined in claim 20 wherein the at least an internal memory block comprises a column and bank decoder.

22. *(Original)* A self-timed memory as defined in claim 21 wherein the at least an internal memory block comprises a precharge and discharge circuitry.

23. *(Original)* A self-timed memory as defined in claim 22 wherein the at least an internal memory block comprises input/output latches.

24. *(Original)* A self-timed memory as defined in claim 23 comprising test circuitry in signal communication with the test system, the test circuitry for providing a control signal to the test system and for providing the external clock signal to the test system during test mode.